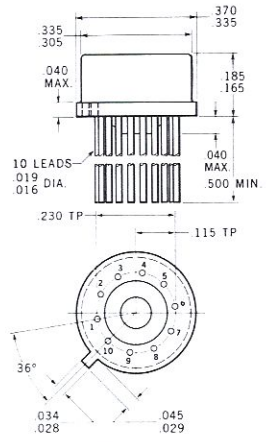
3300
25 BIT STATIC SHIFT REGISTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION—The 3300 is a 25 bit Static Shift Register. It is a monolithic integrated circuit utilizing Planar II*, P-channel enhancement mode MOS technology. Input and output access is made available in 16, 8 and 1 bit increments. This device was designed for use in single phase clock sequential digital systems as a delay line or memory element.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at $T_A = 25°C$	200 mW
Voltage On Clock, Inputs and Supply Pins	−35 V to +0.3 V

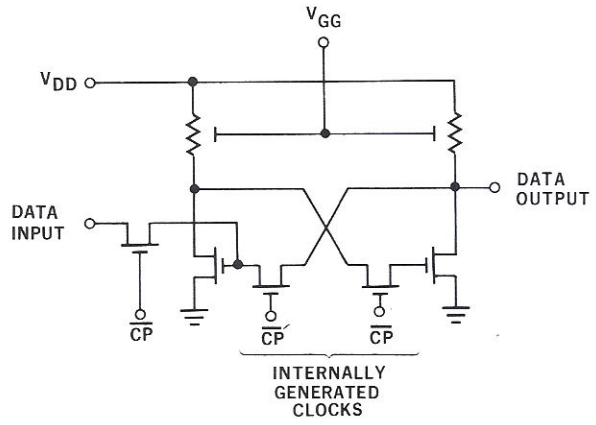
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO–100)



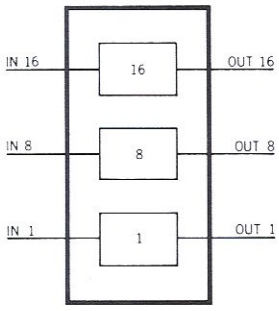
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER CODE A5F330014X

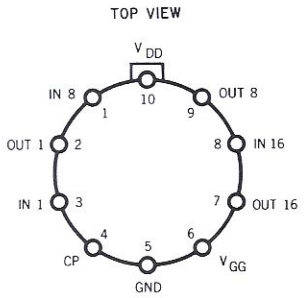
SCHEMATIC DIAGRAM
(ONE BIT)



BLOCK DIAGRAM



CONNECTION DIAGRAM



*Planar is a patented Fairchild process.

NOTE: These ratings are limiting values above which the serviceability of the device may be impaired.

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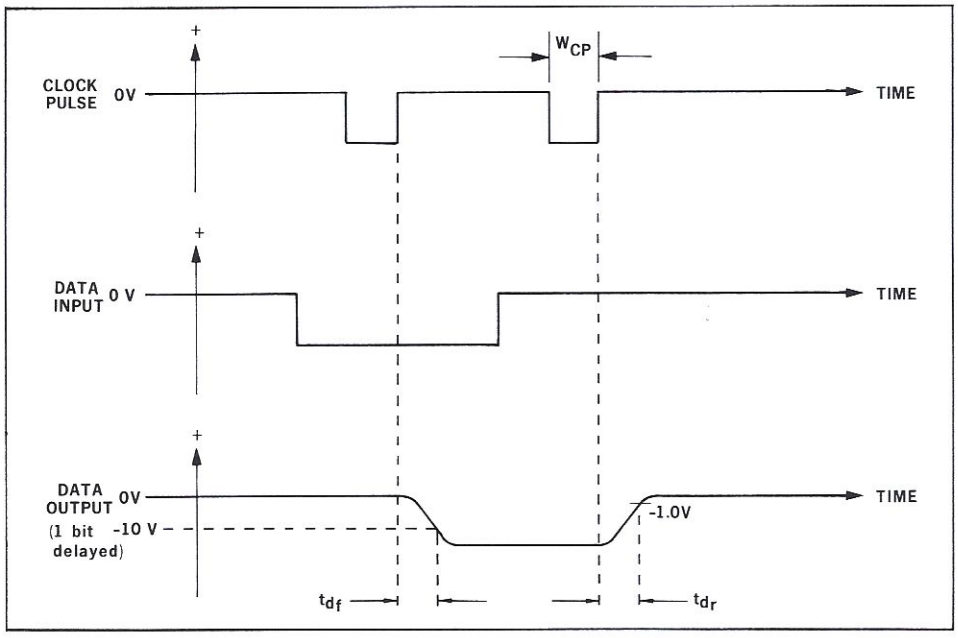
FAIRCHILD MOS INTEGRATED CIRCUIT 3300

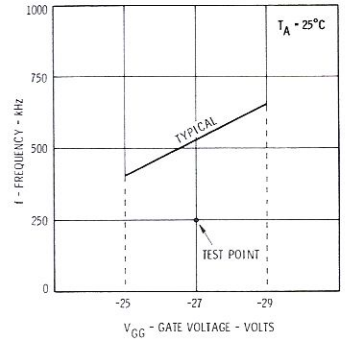
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, V_{GG} (Pin 6) $= -27 \pm 2$ V, V_{DD} (Pin 10) $= -13 \pm 2$ V, unless otherwise specified)

SYMBOL	CHARACTERISTICS		MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
	Power Consumption			50		mW	$V_{clock} = 0$ V
	Operating Frequency		0		250	kHz	$V_{GG} = -27$ V
V_{CP}	Clock Pulse Amplitude	"0" level			−2.0	Volts	
		"1" level	−9.0			Volts	
W_{CP}	Clock Pulse Width		1.0		100	μs	
	Clock Pulse Rise and Fall Time				10	μs	
	Clock Capacitance			3.0		pF	$V_{CP} = 0$ V
I_{CL}	Clock Leakage Current				−1.0	μA	$V_{CP} = -20$ V
V_{IL}	Input Amplitude	"0" level			−2.0	Volts	
V_{IH}		"1" level	−9.0			Volts	
C_{in}	Input Capacitance			2.5		pF	$V_{in} = 0$ V
I_{IL}	Input Leakage Current				−1.0	μA	$V_{in} = -20$ V
V_{OL}	Output Levels	"0" level			−1.0	Volts	$I_{out} = -10$ μA
V_{OH}		"1" level	−10			Volts	$I_{out} = -10$ μA
t_{df}	Time Delay-Fall			1.0		μs	
t_{dr}	Time Delay-Rise			1.2		μs	

TIMING DIAGRAM



TYPICAL OPERATING FREQUENCY VERSUS GATE VOLTAGE



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